Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **CAP+**
2. **GND**
3. **CAP-**
4. **V OUT**
5. **LV**
6. **OSC**
7. **V+**
8. **BOOST**

**.078”**

**.072”**

**3**

**7**

**2 1 8**

**4 5 6**

**MASK**

**REF**

**LT7660**

**Top Material: Aluminum**

**Backside Material: Silicon**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V+**

**Mask Ref: LT7660**

**APPROVED BY: DK DIE SIZE .072” X .078” DATE: 9/28/16**

**MFG: LINEAR TECH THICKNESS .015” P/N: LTC1044A**

**DG 10.1.2**

#### Rev B, 7/19/02